Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 40952

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2018

Third Semester

Electronics and Communication Engineering

EC6302 – DIGITAL ELECTRONICS

(Common to Mechatronics Engineering/Robotics and Automation Engineering)

(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. State De Morgan's theorem and mention its use.
2. What is meant by "maxterm" and "true maxterm" ?
3. What is the basic principle used in order to check or generate the proper parity bit in a given code word ?
4. Draw the logic diagram of a 4-bit parallel subtractor.
5. Bring out the difference between synchronous sequential circuits and asynchronous sequential circuits.
6. A binary ripple counter is required to count up to $16{,}383_{10}$. How many Flip-flops are required ? If the clock frequency is 8.192 MHz, what is the frequency at the output of the MSB ?
7. What is memory expansion and why is it required ?
8. A certain memory has a capacity of 32K × 16. How many bits are there in each word ? How many words are being stored and how many memory cells does this memory contain ?
9. Differentiate between an ASM chart and a conventional flow chart.
10. What is dynamic hazard ? When do they occur ?

PART – B (5×13=65 Marks)

11. a) Explain the Tri-State configuration with neat diagram. (13)

(OR)

b) Minimize the following expression : using Tabulation method

$f = \Sigma m(0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)$ (13)

12. a) Implement the following Boolean function using an 8 : 1 multiplexer considering D as the input and A, B, C as selection lines :

$F(A, B, C, D) = AB' + BD + B'CD'$ (13)

(OR)

b) With a neat diagram, explain in detail about the working of a 4-bit look ahead carry adder. Also mention its advantage over conventional adder. (13)

13. a) Explain in detail about the Ring Counter with its logic diagram, state diagram and its sequence table. (13)

(OR)

b) Discuss in detail about the Pulse-Triggered S-R flip flop. Also draw the output waveform of this flip flop and explain it with an example. (13)

14. a) Write the program table to implement a BCD to Excess-3 code conversion using a PLA. (13)

(OR)

b) Explain in detail about the working of bipolar SRAM cell and single transistor DRAM cell with neat sketches. (13)

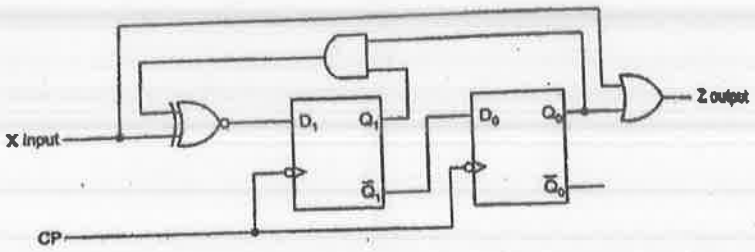
15. a) A clocked sequential circuit with single input x and single output z produces an output z = 1 whenever the input x completes the sequence 1011 and overlapping is allowed :

i) Obtain the state diagram. (5)

ii) Obtain its minimum state table and design the circuit with D flip-flops. (8)

(OR)

b) Draw an ASM chart and the state diagram for the circuit as shown in the figure. **(13)**



PART – C

(1×15=15 Marks)

16. a) Design a J-K counter that goes through states 3, 4, 6, 7 and 3 .... Is the counter self-starting ? Modify the circuit such that whenever it goes to an invalid state it comes back to state 3. **(15)**

(OR)

b) A staircase light is controlled by two switches, one is at the top of the stairs and the other at the bottom of the stairs :

i) Make a truth table for this system.

ii) Write the logic equation in the SOP form.

iii) Realize the circuit using AOI logic.

iv) Realize the circuit using minimum number of (A) NAND gates and (B) NOR gates. **(15)**

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